AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An apparatus, comprising:

two or more memories, wherein each memory has an intelligence wrapper bounding ~~that~~ the memory;

a processor to initiate a Built in Self Test for the memories; and

a serial bus coupled between the processor and each memory; wherein the processor loads a ~~command~~ plurality of commands via the serial bus into a first one of the intelligence wrappers, wherein ~~the command~~ each of the commands comprises representations of a single march element and other data and wherein the first intelligence wrapper contains control logic to decode the command from the processor and to execute a set of test vectors of a march algorithm having a plurality of march elements, on a bounded memory.

2. (Canceled).

3. (Currently Amended) The apparatus of claim 1, wherein the command containing representations of the march element and data is coded in a compressed format and ~~a~~ the first intelligence wrapper comprises control logic that is configured to expand the representation of the march element and the data.

4. (Original) The apparatus of claim 3, wherein the control logic comprises a state machine configured to decode the command and to execute a set of test vectors.

5. (Original) The apparatus of claim 2, wherein a state machine expands the representations of march elements and data in the command to their full-uncompressed form.

6. (Currently Amended) The apparatus of claim 5, wherein the representation comprises a cipher that ~~can be~~is looked up in a data table of the first intelligence wrapper to determine the uncompressed bits and operations that correspond to the compressed information.

7. (Original) The apparatus of claim 1, wherein the two or more memories share the processor.

8. (Original) The apparatus of claim 1, wherein logic contained in the intelligence wrapper operates at a clock speed asynchronous to a clock speed of the processor.

9. (Original) The apparatus of claim 1, wherein the command further comprises:

input data, expected output data, and address information on where to apply data to addresses in the memories.

10. (Original) The apparatus of claim 1, wherein a structure of the command comprises various blocks of interrelated information.

11. (Currently Amended) The apparatus of claim 1, wherein a structure of the command comprises a series of bits and a position of a bit within the series of bits associates that bit with a particular section of information wherein the command includes a section representing the memory address being tested, a section representing the direction of a march algorithm, a section representing the number and type of test operations to be performed, and a section representing expected test data.

12. (Currently Amended) An apparatus, comprising:

two or more memories, each memory has an intelligence wrapper bounding ~~that~~ the memory; ~~and~~

a serial bus; and

a processor to initiate a Built In Self Test for the memories via the serial bus, wherein a first intelligence wrapper contains control logic to decode a compressed command from the processor and to execute a set of test vectors on a bounded memory, wherein the processor sends a command based self test to the first intelligence wrapper at a first speed and the control logic executes the operations associated with ~~that~~ the command at a second speed asynchronous with the first speed, and wherein the processor loads a plurality of commands via the serial bus into the first intelligence wrapper, wherein each of the commands comprises representations of a single march element and other data and wherein the first intelligence wrapper contains control logic to decode the command from the processor and to execute a set of test vectors of a march algorithm having a plurality of march elements, on a bounded memory.

13. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper operates at a clock speed greater than the clock speed of the processor.

14. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper further comprises data comparison logic configured to compare actual vectors at an output of a first bounded memory.

15. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper further comprises address generation logic to generate coordinates of a memory word line to be tested.

16. (Currently Amended) The apparatus of claim 12, wherein the logic in the intelligence wrapper further comprises data generation logic to expand a representation of data input from the processor to generate a sequence of data to be tested for ~~that particular~~the memory.

17. (Original) The apparatus of claim 12, wherein logic in the intelligence wrapper further comprises a state machine configured to decompress the command sent from the processor.

18. (Original) The apparatus of claim 12, wherein a march element in the command may instruct logic in the intelligence wrapper to conduct two or more operations back to back.

19. (Original) The apparatus of claim 1, wherein less than seven routing paths for self test purposes exist between the processor and the bounded memory to be tested.

20. (Canceled).

21. (Currently Amended) A machine readable medium that stores data representing an integrated circuit, comprising:

two or more memories, each memory has an intelligence wrapper bounding ~~that~~ the memory;

a serial bus; and

a processor to initiate a Built In Self Test for the memories via the serial bus, wherein a first intelligence wrapper contains control logic to decode a compressed command from the processor and to execute a set of test vectors on a bounded memory, wherein the processor sends a command based self test to the first intelligence wrapper

at a first speed and the control logic executes the operations associated with ~~that~~ the command at a second speed asynchronous with the first speed, and wherein the processor loads a plurality of commands via the serial bus into the first intelligence wrapper, wherein each of the commands comprises representations of a single march element and other data and wherein the first intelligence wrapper contains control logic to decode the command from the processor and to execute a set of test vectors of a march algorithm having a plurality of march elements, based on the single march element within the command, on a bounded memory.

22. (Original) The machine-readable medium of claim 21, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the memories and the processor.

23. (Canceled).

24. (Original) The machine readable medium of claim 22, wherein less than seven routing paths for self test purposes exist between the processor and the bounded memory to be tested.

25. (Currently Amended) A method, comprising:

compressing information, to be used in a self test of a memory embedded on a chip, into a command, wherein there is a march algorithm representation in said command; ~~and~~

communicating the ~~compressed information~~command via a serial bus to logic bounding the memory; and

receiving the communicated command and expanding the compressed information by the logic bounding the memory, to perform a march algorithm as part of the self-test on the memory.

26. (Canceled).

27. (Original) The method of claim 25, further comprising:

performing operations of the self-test asynchronously with the communication of the compressed information.

28. (Currently Amended) An apparatus, comprising:

means for compressing information, to be used in a self test of a memory embedded on a chip, into a command, wherein there is a march algorithm representation in said command; ~~and~~

means for communicating the ~~compressed information~~command via a serial bus to logic bounding the memory; and

means for receiving the communicated command and expanding the compressed information by the logic bounding the memory, to perform a march algorithm as part of the self-test on the memory.

29. (Canceled).

30. (Original) The apparatus of claim 28, further comprising:

means for performing operations of the self-test asynchronously with the communication of the compressed information.